REMARKS

In the Office Action dated December 1, 2004, the Examiner rejected claims 35, 37-39, 45, 47-49, 63 and 65-70. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

The Examiner rejected claims 35, 37-39, 45, 47-49, 63 and 65-67 under § 103(a) as being unpatentable over Pai (U.S. Patent No. 6,503,776) in view of Huang (U.S. Patent No. 6,753,206). Further, the Examiner rejected claims 68-70 under § 103(a) as being unpatentable over Pai (U.S. Patent No. 6,503,776) in view of Hakey (U.S. Patent No. 6,627,477) or Moden (U.S. Patent No.6,512,303). The Examiner's rejections are too lengthy to be reproduced efficiently herein. However, Applicants respectfully traverse the Examiner's rejections.

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

The present application relates generally to semiconductor processing and, more particularly to an integrated circuit comprising a die stack coupled to a substrate. More particularly, independent claims 35, 45 and 63 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die, and "wherein each die in the stack of at least two semiconductor is functional." Independent claims 38, 48 and 66 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die, and "wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack." Independent claims 68, 69 and 70 each recite an integrated circuit comprising a stack coupled to a substrate wherein the stack comprises at least two semiconductor die, and "wherein each die in the stack is successively

thinner than the previous die." Based on the similarity in the recited subject matter, the rejections will be discussed in accordance with the claim groupings set forth in this paragraph.

Claims 35, 45 and 63

Claims 35, 45 and 63 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein each die in the stack of at least two semiconductor die is functional." In contrast, the Pai reference discloses a die stack where a part of the stack includes a "dummy chip" with film adhesive that adheres to other die within the stack. Col. 3, line 65 – Col.4, line 5. The dummy chip is a die similar to the other die in the stack, but the dummy chip does not include wiring "because it is not employed in the device operation." Col. 3, lines 20-22. In other words, the dummy chip in the stack disclosed in the Pai reference is non-functional. Accordingly, the Pai reference fails to teach or suggest a die stack wherein each of the die in the stack is functional as recited in the present claims.

In his rejection, the Examiner stated:

> Pai teaches a dummy die, the dummy die serving a function, thus being functional. The instant specification teaches that each die is tested to be functional, and in light of the specification, the Examiner believes that Pai reads on this limitation of being functional.

As discussed in the present specification, one of the disadvantages of prior stacking techniques is that damaged die may unknowingly be incorporated into a stacked package. Page 10, lines 7-9. In accordance with embodiments of the present invention, prior to attachment of the stack to a substrate, each of the die may be tested to ensure that all die in the stack are

functional, thus forming a known good die stack (KGDS). Page 12, lines 10-12. Applicants respectfully submit that in light of the present specification, it is clear that a "functional" die refers to an electrically functional die. Applicants further assert that those skilled in the art presented with the term "functional die" would certainly understand the term to refer to "electrically functional die." While the Examiner is correct in asserting that the dummy die of the Pai reference does indeed have a function, those skilled in the art would not interpret the dummy die disclosed in the Pai reference as a "functional die." Accordingly, Applicants respectfully submit that interpreting the dummy die of the Pai reference as "functional" simply because it does something or has a function is an unreasonably broad interpretation of the claim, since those skilled in the art would not make such a correlation.

Indeed, despite the Examiner's assertions regarding the functionality of the dummy die disclosed in the Pai reference, the Examiner goes on to cite the Huang reference and states that "Huang forms a stack similar to that of Pai, but teaches a stack where all die are 'electrically' functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang." While the Examiner asserted that the dummy die of the Pai reference is functional and thus that this limitation of the present claims is disclosed in the Pai reference, the Examiner then cites Huang as disclosing this particular limitation.

With regard to the Huang reference, Applicants respectfully submit that those skilled in the art would not be motivated to combine the Pai and Huang references, much less combine the references in the manner recited in the present claims. The Huang reference discloses a dual-chip

integrated circuit package. "The dual-chip integrated circuit package includes a lead frame having a first set of leads and a second set of leads...in which the first integrated circuit chip is mounted on one side of the inner part of the first set of leads, and the second integrated circuit chip is mounted on the other side of the same..." Abstract. Accordingly, the Huang reference simply discloses coupling a first integrated circuit chip to the first side of a set of leads and coupling a second integrated circuit chip to the other side of a set of leads. As will be appreciated by those skilled in the art, lead frame technology is vastly different from technology related to packages incorporating a chip coupled to a substrate. Indeed, as discussed throughout the present specification, coupling a die or a die stack to a substrate may present certain challenges due to a mismatch in coefficients of thermal expansion of the die and the substrate. "The substrates on which the die are stacked generally have a different coefficient of thermal expansion." Page 3, lines 18-20. "Thus once the stack is formed on the substrate and cured as in typical die stacking systems, a mismatch in the coefficients of thermal expansion (CTEs) may be introduced, which may cause cracking or other problems with the die stack since the interface between each of the die and the interface between the die and the substrate are being cured at the same time but have different CTEs." Page 3, line 20 – page 4, line 1. Applicants provide this text as an example in support of the contention that those skilled in the art simply would not look to techniques for coupling die to lead frames as in the Huang reference, to modify integrated circuit packages where die are attached to substrates as in the Pai reference. Though the Huang reference does indeed illustrate a first functional die attached to one side of the lead frame and a second functional die attached to a second side of the lead frame, there is absolutely no motivation from

this reference to stack two functional die together and then attach them to a substrate in the manner recited in the present application.

Further, Applicants are unaware of how one skilled in the art could modify the package disclosed in the Pai reference in view of the Huang reference to achieve the recited integrated circuit package. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959); see M.P.E.P. § 2143.01. The Pai reference discusses perceived problems associated with multi-chip stacked packages including die attached directly to a substrate and stacked directly on top of each other. See background. To solve problems such as bond line thickness and CTE mismatch, the Pai reference teaches introducing a dummy die (i.e., a die which is not electrically functional) between functional die. Though Applicants do not know how one would modify the integrated circuit package of Pai in view of the integrated circuit package of Huang, assuming *arguendo* that such a modification could be made, this would destroy the principle of operation taught by the Pai reference. That is, the Pai reference explicitly teaches inserting a dummy die between functional die to create a consistent bond line. One skilled in the art would not be motivated to modify the Pai reference by removing the dummy die since it would destroy the principle of operation as taught by the Pai reference by reintroducing the inconsistent bond line thickness and the problems associated with CTE mismatch.

For at least the reasons set forth above, Applicants respectfully submit that claims 35, 45 and 63, as well as those claims dependent thereon, are not rendered obvious by the cited combination. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 35, 45 and 63, as well as those claims dependent thereon.

Claims 38, 48 and 66

Claims 38, 48 and 66 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack." As described in the present specification, as amended, Figs. 5C and 5D are cross-sectional views of "shingle stacks." Page 14, line 10. Shingle stacks are die stacks wherein upper die may overhang die below them in the stack such that their centers are not aligned. Page 14, lines 11-12. Contrary to the Examiner's assertion, the Huang reference does not disclose a shingle stack as reasonable interpreted in light of the present specification. That is to say that the Huang reference does not disclose a die stack wherein an upper die overhangs a lower die. Even if the integrated circuit package disclosed in the Huang reference could be fairly characterized as a die stack, the upper die *does not* overhang the die below. The upper die does not "overhang" anything. As clearly illustrated in Fig. 2 of the Huang reference, the upper die is adhered directly and completely to a lead frame. Thus, no portion of the upper die overhangs anything. Accordingly, neither of the cited references, either alone or in combination, discloses all of the features recited in claims 38, 48 and 66.

Because the cited references, taken alone or in combination, fail to disclose each of the features recited in claims 38, 48 and 66, Applicants respectfully submit that the cited combination cannot possibly render the recited subject matter obvious. Further, as discussed in detail above with regard to the rejections of claims 35, 45 and 63, there is simply no suggestion to combine the cited references in the manner recited in the present claims. For this additional reason, Applicants respectfully submit that the cited combination cannot possibly render the recited subject matter obvious. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 38, 48 and 66 as well as those claims dependent thereon.

Claims 68, 69 and 70

Claims 68, 69 and 70 each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein each die in the stack of at least two die is successively thinner than the previous die." The Examiner cited the Pai reference in combination with either Hakey or Moden. The Hakey reference discloses a method of achieving coplanarity between chips. Col. 4, lines 62-63; Fig. 6. While it is true that the Hakey reference discloses chips 12 of the varying thicknesses in the Z-axis, these chips are attached directly to a substrate 10. See Fig. 3. That is to say, each of the chips 12 are positioned directly adjacent to one another, not on top of one another. Applicants respectfully submit that there is absolutely no motivation provided in either the Pai reference or the Hakey reference that would suggest using the die of varying thickness as provided in the direct mount package disclosed in the Hakey reference with the die stack of the Pai reference.

As repeatedly discussed throughout the Hakey reference, the reference is directed specifically to aligning the chips 12 adjacent to one another such that the active surface of the devices are co-planar. See e.g. Abstract; Fig. 6. Because the Hakey reference is directed to ensuring that each of the active surfaces on the chips 12 are co-planar, the reference actually teaches away from forming a die stack. A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997). In fact, teaching away from the art is a *per se* demonstration of lack of *prima facie* obviousness. *In re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529 (Fed. Cir. 1988). Accordingly, it is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983); M.P.E.P. § 2145. The co-planar design of the Hakey reference cannot be maintained if the die are stacked. Because the Hakey reference actually teaches away from combining it with the Pai reference, the references cannot possibly be combined to render the recited subject matter obvious.

With regard to Moden, the Moden reference discloses a package comprising a semiconductor die 12 coupled to an adapter board 18 which is then coupled to a master board 30. Col. 4, lines 13-32. As explicitly stated in the Moden reference, the "adapter board" is a printed circuit board or substrate. Col. 3, lines 7-10. Applicants assume that the Examiner is applying the semiconductor die 12 and the adapter board 18 of the Moden reference to illustrate a die stack "wherein each die in the stack of at least 2 die is successively thinner than the previous die." However, it is clear that the Moden reference only discloses a package having a single

semiconductor die 12. It is clear that the adapter board 18 disclosed in the Moden reference is *not* a semiconductor die. Therefore, the thickness of the adapter board 18 is irrelevant. The Moden reference does not disclose a stack of successively thinner die. For at least this reason, neither the Hakey reference nor the Moden reference, taken alone or in combination discloses each of the elements recited in claims 68, 69 and 70, much less provides any suggestion to combine these references in the manner recited in the present claims. Accordingly, the cited combination cannot possibly render the recited subject matter obvious. Therefore, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 68, 69 and 70.

Claims 35, 38 and 68

Claims 35, 38 and 68 each recite an integrated circuit comprising a die stack coupled to a substrate, "each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature," and wherein the stack is coupled to a substrate by a second adhesive, "the second adhesive being curable at a second temperature lower than the first temperature."

In rejecting claims 35, 38 and 68, the Examiner stated:

> [i]t is noted that Pai teaches this (Col. 3, lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The Patentability of a product does not depend on its method of production. MPEP 2113.

While Applicants agree with the Examiner's statement regarding the patentable weight of process limitations in a product-by-process claim, Applicants respectfully traverse the Examiner's assertion that these claims are in fact product-by-process claims. As stated above, the claims recite a first adhesive "being *curable* at a first temperature," and a second adhesive "being *curable* at a second temperature lower than the first temperature." Emphasis added. The present claims do not recite an actual act of curing the adhesive. In contrast, the present claims recite physical qualities of each of the first and second adhesives. That is, the first adhesive is "curable at a first temperature," and the second adhesive is "curable at a second temperature." For instance, the first adhesive used in the die stack may have properties such that it is curable at a high temperature, such as in the range of 50-400° C, for example. Page 12, lines 8-9. The adhesive used to attach each die together may be different than the adhesive which may be used later to attach the die to the substrate. Page 12, lines 12-14. The second adhesive may be curable at a second temperature such as in the range of 50-100° C, for example. As will be appreciated by those skilled in the art, in order for the adhesives to be curable at different temperatures, the adhesives have different physical qualities. Accordingly, Applicants respectfully submit that these structural limitations should indeed be given patentable weight.

Conclusion

In view of the remarks set forth above, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 35, 37-39, 45, 47-49, 63, and 65-70. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefore. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0078-1/FLE (01-0752.01).

Respectfully submitted,

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